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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/620,140	07/20/2000	David A. Zimlich	2146-12	2828

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EXAMINER
NGUYEN, JENNIFER T

ART UNIT	PAPER NUMBER
2674	

DATE MAILED: 12/17/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/620,140	Applicant(s) ZIMLICH, DAVID A.	
	Examiner Jennifer T Nguyen	Art Unit 2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 July 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This office action is responsive to amendment filed on 10/23/2002.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 2, 5-11, 15-19, 21, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakuragi et al. (U.S. Patent No. 6,195,076) in view of Shimizu (U.S. Patent No. 6,201,529).

Regarding claims 1, 9, and 18, referring to Fig. 4, Shakuragi teaches a driver circuit for driving signal lines of a matrix type display device comprising: pulsewidth modulation circuitry (8) for generating pulsewidth modulated video data; and driver circuitry (Dy1-Dyn) for driving said signal lines in accordance with the pulsewidth modulated video data (col. 1, lines 7-12, lines 26-19 and col. 11, lines 29-32).

Shakuragi differs from claims 1, 9, and 18 in that he does not specifically teach latching the pulse width modulated video data and driving said signal lines in accordance with the latched data. However, referring to Fig. 5, Shimizu discloses latching (406) the pulse width modulated video data (401) (i.e. PWM signal) and driving said signal lines in accordance with the latched data (col. 7, lines 30-34, col. 9, lines 48-49). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the latching as taught

by Shimizu in the system of Shakuragi in order to provide stable of the current flow to the emitters that is selectively controlled to produce a desired image.

Regarding claims 2 and 10, referring to Fig. 7, Sakuragi further teaches the driver circuitry comprises level-shifting circuits (21) (col. 14, lines 65-67).

Regarding claims 5 and 19, Sakuragi further teaches the driver circuit wherein said signal lines are connected to emitter elements of a field emission display (from col. 13, line 64 to col. 14, lines 12 and lines 7-11).

Regarding claims 6, 15, and 21, referring to figures 12A and 12B, Sakuragi further teaches the driver circuit wherein said pulsewidth modulation circuitry generates the pulsewidth modulated video data based on RGB video data supplied thereto (col. 15, lines 41-45).

Regarding claims 7 and 16, the combination of Sakuragi and Shimizu differs from claims 7 and 16 in that it does not teach the driver circuitry is provided on a chip other than a chip on which said pulsewidth modulation circuitry is provided. However, it would have been obvious to obtain the driver circuitry is provided on a chip other than a chip on which said pulsewidth modulation circuitry is provided in order to simplify the design of the driver circuit and easy to upgrade and repair the circuit.

Regarding claims 8 and 17, Sakuragi teaches the driver circuit wherein said driver circuitry comprises driver circuits that are loaded in parallel with the pulsewidth modulated video data (see figure 4).

Regarding claim 11, Sakuragi further teaches the matrix type display device wherein said display device is a field emission display device (col. 1, lines 16-17).

Regarding claim 22, Shakuragi differs from claim 22, in that he does not specifically teach latch circuits for latching the pulsewidth modulated video data. However, referring to Fig. 5, Shimizu discloses latch circuit (406) for latching the pulse width modulated video data (401) (i.e. PWM signal) and driving said signal lines in accordance with the latched data (col. 7, lines 30-34, col. 9, lines 48-49). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the latch circuit as taught by Shimizu in the system of Shakuragi in order to provide stable of the current flow to the emitters that is selectively controlled to produce a desired image.

4. Claims 3, 4,13, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakuragi et al. (U.S. Patent No. 6,195,076) in view of Shimizu (U.S. Patent No. 6,201,529) and further in view of Mosier (U.S. Patent No. 6,353,425).

Regarding claims 3, 4, 13, and 14, the combination of Sakuragi and Shimizu differs from claims 3, 4, 13 and 14 in that it does not specifically teach pulsewidth modulation circuitry comprises a programmable logic array and ASIC. However, referring to Fig. 3, Mosier discloses arrangement circuit (100) comprises a programmable logic array and ASIC (col. 5, lines 40-45). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the arrangement circuit comprises a programmable logic array and ASIC as taught by Mosier in the system of the combination of Sakuragi and Shimizu in order to simplify the circuitry and save space, reduce size, weight and costs.

5. Claims 12 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakuragi et al. (U.S. Patent No. 6,195,076) in view of Shimizu (U.S. Patent No. 6,201,529) and further in view of Wood (U.S. Patent No. 6,288,695).

Regarding claims 12 and 20, the combination of Sakuragi and Shimizu differs from claims 12 and 20 in that it does not specifically teach the display device is a plasma display device. However, Wood discloses a display device is a plasma display device (col. 1, lines 60-65). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the plasma display device as taught by Wood in the system of the combination of Sakuragi and Shimizu in order to provide a matrix display type having a large screen and high resolution.

6. Claims 23-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakuragi et al. (U.S. Patent No. 6,195,076) in view of Shimizu (U.S. Patent No. 6,201,529) and further in view of Hashimoto (U.S. Patent No. 6,014,122).

Regarding claim 23, the combination of Sakuragi and Shimizu differs from claim 23 in that it does not specifically teach a single latch circuit is provided for each signal line. However, referring to Fig. 2, Hashimoto discloses a single latch circuit (142) is provided for each signal line (Y1). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the a single latch circuit is provided for each signal line as taught by Hashimoto in the system of the combination of Sakuragi and Shimizu in order to provide an suitable output for each signal line.

Regarding claim 24, the combination of Sakuragi and Shimizu differs from claim 24 in that it does not specifically teach a data buffer whose outputs are selectively latched into said latch circuits in accordance with latch enable signals. However, referring to Fig. 1, Hashimoto discloses a data buffer (19) whose outputs are selectively latched into said latch circuits (12) in accordance with latch enable signals (col. 3, lines 40-66). Therefore, it would have been obvious

to one of ordinary skill in the art at the time the invention was made to incorporate the data buffer as taught by Hashimoto in the system of the combination of Sakuragi and Shimizu in order to allow to select suitable signals for the latch circuit.

Regarding claim 25, the combination of Sakuragi, Shimizu, and Hashimoto teaches output transistors include series connected N-channel and P-channel transistors associated with each signal line, wherein an output of a corresponding latch circuit is supplied to a control terminal of one of the N-channel and P-channel (col. 4 of Hashimoto, lines 8-28, col. 10, lines 20-28).

7. Applicant's arguments with respect to claims 1-21 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Jennifer T. Nguyen** whose telephone number is **703-305-3225.** The examiner can normally be reached on Mon-Fri from 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Richard A Hjerpe** can be reach at **703-305-4709**.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, DC. 20231

Or faxed to: 703-872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, sixth-floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is 703-306-0377.

Jennifer T. Nguyen
Patent Examiner
Art Unit 2674

RICHARD HJERPE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600